

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Case Docket No. YKI-0049

The Assistant Commissioner of Patents  
Washington, D.C. 20231"Express Mail" mailing label number EL 564090268US

Date of deposit September 27, 2000

I hereby certify that this paper or fee is being deposited with the  
United States Postal Service "Express Mail Post Office to Address"  
service under 37 CFR 1.10 on the date indicated above and is  
addressed to the Commissioner of Patents and Trademarks,  
Washington, D.C. 20231.

Jennifer Matson

(Typed or printer name of person mailing paper or fee)

*Jennifer Matson*

Sir:

Transmitted herewith for filing is the patent application of :

INVENTOR(S): NAOAKI KOMIYA, ET AL.

FOR: ACTIVE MATRIX TYPE ELECTROLUMINESCENCE DISPLAY DEVICE

Enclosed are:

☒ 12 pages of specification.☒ 5 claims.☒ 2 sheet(s) of drawing(s).☒ Declaration and Power of Attorney☐ Information Disclosure Statement.☐ An associate power of attorney.☒ An assignment of the invention to Sayno Electric Co., Ltd.☐ A certified copy of a Patent Application No. \_\_\_\_\_☐ A verified statement to establish small entity under 37 CFR 1.9 and 37 CFR 1.27.

The filing fee has been calculated as shown below:

			SMALL ENTITY		LARGE ENTITY	
FOR:	# FILED	# EXTRA	RATE	FEE	RATE	FEE
BASIC FEE	////////	////////	\$345	\$345	\$690	\$690.00
TOTAL CLAIMS (20)	5	0	X 9		x 18	
INDEP. CLAIMS (3)	1	0	x 39		x 78	
MULTIPLE DEPENDENT CLAIMS	0	0	+130		+260	
			TOTAL	\$	TOTAL	\$690.00

JC849 U.S. PTO  
09/27/00JC849 U.S. PTO  
09/27/00

09/27/00

09571843-092700

☐ Please charge my Deposit Account # **06-1130** the amount of \$ . A duplicate copy of this sheet is enclosed.

☒ A check in the amount of \$690.00 to cover the filing fee is enclosed.

☒ A check in the amount of \$40.00 to cover recordation of the assignment is enclosed.

☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account **06-1130**.

☒ Any additional filing fees required under 37 CFR 1.16.

☒ Any patent application processing fees under 37 CFR 1.17.

Please file this application and conduct all future correspondence with Applicants' attorney identified below.

Respectfully Submitted,

NAOAKI KOMIYA, ET AL.

Applicants' Attorney

By: 

David A. Fox  
Registration No. 38,807  
Customer No. 23413

Date: September 27, 2000

09671843-092700

## ACTIVE MATRIX TYPE ELECTROLUMINESCENCE DISPLAY DEVICE

## BACKGROUND OF THE INVENTION

## 1. Field of the Invention

5 The present invention relates to an active matrix type EL display device with display pixels including an electroluminescence element (hereinafter referred to as an EL element) and a thin film transistor arranged in a matrix form, and particularly to an art for stably illuminating each display pixel preventing select signals in gate signal lines connected to and shared by the display pixels from being delayed.

## 2. Description of the Related Art

10 EL elements have various advantages, including, because they are self illuminating elements, an obviated need for a backlight as required in liquid crystal display devices and unlimited viewing angle. Because of these advantages, it is widely expected that EL elements will be use in the next generation of display devices.

15 Two basic methods are known for driving EL elements. One of these is called a simple, or passive, matrix type, with the other, which employs a thin film transistor as a switching element, is known as an active matrix type. The active matrix type does not suffer from cross talk between the column and row electrodes, which is a problem known in the simple matrix type. Moreover, because 20 the EL elements are driven with a lower current density, a high luminescence efficiency can be expected.

25 Fig. 3 is a circuit diagram schematically showing an active

matrix type EL display device. In the figure, the display pixels GS1, GS2, GS3, ... GSj are arranged in one row. One display pixel GS1 includes an organic EL element 11, a first thin film transistor 12 (an N channel type transistor) acting as a switching element in which a display signal DATA1 is applied to the drain and which is switched on and off in response to a select signal SCAN, a capacitance 13 which is charged by the display signal DATA1 supplied when the first thin film transistor 12 is switched on and which maintains a maintenance voltage Vh when the first thin film transistor 12 is switched off, and a second thin film transistor 14 (a P channel type transistor), with its drain connected to a drive supply voltage Vdd and its source connected to the anode of the organic EL element 11, for driving the organic EL element when the maintenance voltage Vh is supplied from the capacitance 13 at the gate.

The other display pixels GS2, GS3, ... GSj have an equivalent structure. Although the display pixels are also arranged in the column direction, this arrangement is not shown in order to simplify the drawing. Reference numeral 15 represents a gate signal line which is connected to and shared by each of the display pixels GS1, GS2, GS3, ... GSj for supplying a select signal SCAN. Reference numeral 16 represents a gate drive circuit for supplying the select signal SCAN to the gate signal line.

The select signal SCAN becomes H level during a selected one horizontal scan period (1H), and the first thin film transistor 12 is then switched on based on the select signal. Next, a display signal DATA1 is supplied to one end of the capacitance 13 and the

capacitance 13 is charged with a voltage  $V_h$  corresponding to the display signal DATA1. The voltage  $V_h$  is maintained in the capacitance 13 for a period of one vertical scan period (1V) even after the first thin film transistor 12 is switched off due to the select signal SCAN becoming L level. Because this voltage is supplied to the gate of the second thin film transistor 14, the second thin film transistor 14 becomes continuous in response to the voltage  $V_h$  and the organic EL element 11 is illuminated.

However, in larger size conventional EL display devices, differences in luminance throughout the display device have been observed.

The gate signal line 15 is formed from chrome evaporated on a glass substrate, in consideration of heat endurance and ease of processing. Because the gate signal line 15 is extended on the display region in order to be connected to and shared by each of the display pixels GS1, GS2, GS3, ... GSj, a resistance and a floating capacitance are inevitably generated. For example, in an active matrix type EL display device having a number of pixels of 220 x 848, the resistance value of one gate signal line 15 is approximately 320  $\Omega$  and the floating capacitance is approximately 20 pf. The resistance and floating value increase as the number of pixels increases.

Therefore, due to signal transmission delay, it is difficult to sufficiently increase the signal level to H level at the further end of the gate signal line 15 which is far apart from the gate drive circuit 16 when supplying a select signal SCAN of H level to the gate signal line 15 based on the select signal SCAN. It

is found that due to this insufficient voltage increase in signal line, the signal level of a display signal DATAn cannot be fully transferred to the capacitance 13 at display pixels in the end section, causing a decrease in the illuminating luminescence of the organic EL element, and therefore, the overall luminescence of the display device becomes unstable.

#### SUMMARY OF THE INVENTION

The present invention stabilizes luminance among the display pixels by minimizing delay in the select signal SCAN on the gate signal line connected to and shared by each of the display pixels.

According to one aspect of the present invention, there is provided an active matrix type EL display device comprising a plurality of display pixels arranged in a matrix form in rows and columns, gate signal lines each of which is connected to and shared by a plurality of display pixels provided for each row, and gate drive circuits for sequentially supplying select signals to the gate signal lines, wherein, each of the display pixels includes an EL element, a first thin film transistor in which a display signal is applied to the drain and which is switched on and off in response to the select signal, and a second thin film transistor for driving the EL element based on the display signal, and wherein the gate drive circuits are placed so that the select signal is supplied on each of the gate signal lines from both ends of the gate signal lines.

With this structure, because the gate drive circuits are placed to drive each of the gate signal lines from both ends, the

select signal can be more rapidly supplied to the gate signal lines compared to the conventional method, and thus, each of the display pixels can be illuminated at a stable luminance.

5

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a figure illustrating an active type electroluminescence display device according to one embodiment of the present invention.

Fig. 2 is a circuit diagram illustrating a gate drive circuit according to the embodiment of the present invention.

Fig. 3 is a diagram illustrating a conventional active type EL display device.

#### DESCRIPTION OF THE PREFERRED EMBODIMENT

An active matrix type EL display device according to a preferred embodiment of the present invention is described hereinafter referring to Figs. 1 and 2.

Fig. 1 is a circuit diagram schematically showing a structure of an active matrix type EL display device. Display pixels GS11, GS12, GS13, ... GSij, are arranged in rows and columns to form a matrix. Each of the display pixels includes an organic EL element 1, a first thin film transistor 2 in which a display signal DATAj is applied to the drain and which is switched on and off in response to a select signal supplied from a gate signal line GLi, a capacitance 3, and a second thin film transistor 4 for driving the EL element 1 based on the display signal DATAj. One end of the capacitance 3 is connected to a common electrode and biased to a constant voltage

of Vsc.

Fig. 1 shows a full-color EL display device and three types of display pixels are repeatedly arranged, each type of display pixel having an organic EL element illuminating respectively in red (R), green (G), and blue (B). In other words, a common drive voltage source RPVdd is supplied to the display pixels GS11, GS21, GS31, ... GSi1 having organic EL elements illuminating in red, a common drive voltage source GPVdd is supplied to the display pixels GS12, GS22, GS32, ... GSi2, having green illuminating organic EL elements, and a common drive voltage source BPVdd is supplied to the display pixels GS13, GS23, GS33, ... GSi3, for blue illuminating organic EL elements. A monochrome EL display device can be constructed by arranging display pixels of one type in rows and columns.

A display signal DATA1 is applied to the display pixels arranged in the first column such as GS11, GS21, and GS31; a display signal DATA2 is applied to the display pixels arranged in the second column such as GS12, GS22, and GS32; and so on such that a display signal DATAj is applied to the display pixels arranged in the jth column such as GS1j, GS2j, and GS3j.

A common gate signal line GL1 is connected to the display pixels arranged in the first row such as GS11, GS12, and GS13; a common gate signal line GL2 is connected to the display pixels arranged in the second row such as GS21, GS22, and GS23; and so on such that a common gate signal line GLi is connected to the display pixels arranged in the ith row such as GSi1, GSi2, and GSi3.

A characteristic of the present invention is that a pair of



gate drive circuits 5 and 6 are provided to supply a select signal SCAN to each of the gate signal lines such as GL1, GL2, and GL3 from both ends of the respective gate signal line. The gate drive circuits 5 and 6 are placed symmetrically in the right and left directions with respect to the display region. The gate signal lines such as GL1, GL2, and GL3 are connected to and shared by, for example, 848 display pixels. Because the gate signal lines are formed of an evaporated chrome thin film with a line width of approximately  $4\ \mu$ , they have large resistance and floating capacitance values. According to the present invention, any delay of the select signal SCAN transmitted on the gate signal lines such as GL1, GL2, and GL3 can be minimized; the select signal SCAN can be sufficiently increased to H level; and, thus, the illumination intensity of the EL element in the display pixels can be unified. Also, because the signal level of the display signals DATAj can be reliably transmitted to the capacitance 13, a decrease in the luminance of the organic EL element can be prevented.

Fig. 2 is a circuit diagram showing a structure of the gate drive circuits 5 and 6. A reference clock CKV is supplied from outside. A plurality of shift registers SR1 through SR220 are serially connected to sequentially shift the reference clock CKV by one horizontal scan period (1H). The select signal SCAN, which is the output of each of the shift registers, is transmitted to each of the gate signal lines GL1 through GL220 via buffer amplifiers 7.

In other words, each of the select signals SCAN having a pulse width of one horizontal scan period (1H), is shifted by each of

the shift registers SR1 through SR220 and is output sequentially through each of the gate signal lines GL1 through GL220. The number of shift registers provided is 220 to correspond to the number of pixels of 220 x 848 in the active matrix type EL display device in the example of this embodiment. However, the numbers of shift registers and of the buffer amplifiers can be modified to suit and correspond to the number of rows of display pixels.

The active matrix type EL display device is driven as follows. When a gate signal line GL1 is selected by a select signal SCAN, the display pixels in the first row such as GS11, GS21, and GS31 are selected. At this point, because the gate signal line GL1 is driven from both ends, the signal can be quickly increased to the H level.

During one horizontal scan period (1H), display signals DATA1, DATA2, DATA3, ... DATAj are sequentially supplied to each of the display pixels GS11, GS12, GS13, ... GS1j from each of the data lines. The display signals DATA1, DATA2, DATA3, ... DATAj are maintained by a sampling circuit (not shown) and the timing for outputting the signals is controlled via a transfer gate provided for each of the display signal terminals. The EL element 1 in each of the display pixels GS11, GS12, GS13, ... GS1j, is stably illuminated at a luminance corresponding to the respective one of display signals DATA1, DATA2, DATA3, ... DATAi. Similarly, gate signal line GL2 is selected by the next select signal SCAN. These steps are repeated for one vertical scan period (1V).

As described, according to the present invention, by minimizing delay in the select signal on the gate signal line

connected to and shared by each of the display pixels, an active matrix type EL display device in which each pixel electrode illuminates at a stable luminance can be provided.

09674343-092700

WHAT IS CLAIMED IS:

1. An active matrix type electroluminescence display device comprising:

5 a plurality of display pixels arranged in rows and columns in a matrix form;

gate signal lines, each of which is connected to and shared by a plurality of display pixels provided on each row; and

10 gate drive circuits for sequentially supplying select signals to said gate signal lines; wherein

each of said display pixels includes an electroluminescence element, a first thin film transistor in which a display signal is applied to the drain and which is switched on and off in response to said select signal, and a second thin film transistor for driving  
15 said electroluminescence element based on said display signal; and

said gate drive circuits are placed so that said select signals are supplied from both ends of said gate signal lines to said gate signal lines.

20 2. An active matrix type electroluminescence display device according to claim 1, wherein

said gate drive circuits include a first and second gate drive circuits arranged in a symmetric pattern to the right and left of a display region constructed from said plurality of display  
25 pixels.

3. An active matrix type electroluminescence display device

according to claim 2, wherein

each of said first and second gate drive circuits includes a plurality of shift registers for sequentially shifting a reference clock with a pulse width of one horizontal period.

5

4. An active matrix type electroluminescence display device according to claim 3, wherein

each of said first and second gate drive circuits includes buffer amplifiers for driving said gate signal lines based on the output of said shift registers.

10

5. An active matrix type electroluminescence display device according to claim 4, wherein

the number of said shift registers and of the buffer amplifiers included in each of said first and second gate drive circuits corresponds to the number of rows of said plurality of display pixels.

15

## ABSTRACT OF THE DISCLOSURE

An active matrix type electroluminescence display device is provided which comprises a plurality of display pixels GS11, GS12, GS13, arranged in a matrix of rows and columns; gate signal lines GL1, GL2, Gli connected to and shared by a plurality of display pixels arranged in each row; and gate drive circuits for sequentially supplying a select signal SCAN to the gate signal lines GL1, GL2, GL3, Gli. Each display pixel includes an electroluminescence element, a first thin film transistor in which a display signal DATA is applied to the drain and which is switched on and off in response to the select signal SCAN, and a second thin film transistor for driving the EL element based on the display signal DATA. The gate drive circuits are placed so that each of the gate signal lines GL1, GL2, GL3, Gli is driven from both ends.

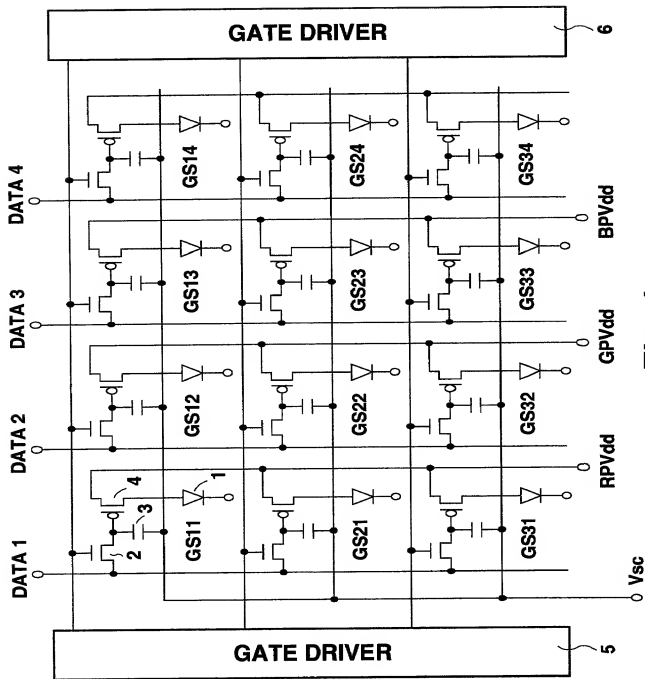
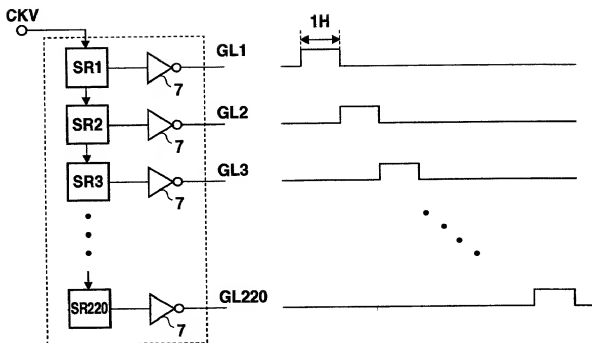
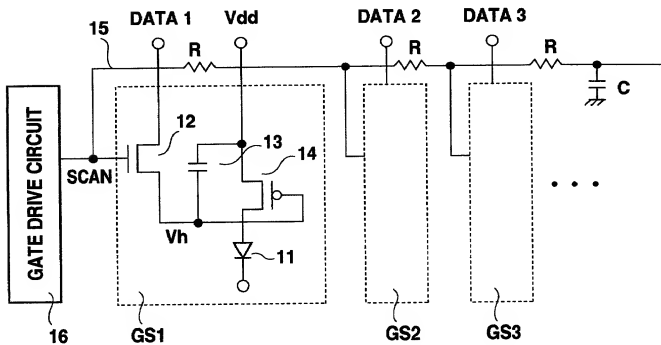


Fig. 1



**Fig. 2**



**Fig. 3 PRIOR ART**



# Declaration and Power of Attorney For Patent Application

## 特許出願宣言書及び委任状

### Japanese Language Declaration

#### 日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、郵便箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ACTIVE MATRIX TYPE  
ELECTROLUMINESCENCE DISPLAY  
DEVICE

上記発明の明細書（下記の欄で×印がついていない場合は、本表に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ 月 日に出発され、米国出願番号または特許協定条約  
国際出願番号を \_\_\_\_\_ とし、  
(該当する場合) \_\_\_\_\_ に訂正されました。

☐ was filed on \_\_\_\_\_  
as United States Application Number or  
PCT International Application Number  
\_\_\_\_\_ and was amended on  
\_\_\_\_\_ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則連邦第 37 編第 1 条 5.6 項に定義されるとおり、特許資格の右態について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

**Japanese Language Declaration**  
(日本語宣言書)

私は、米国法典第 3 5 編 1 1 9 条 (a)-(d) 項又は 3 6 5 条 (b) 項に基づき下記、米国以外の国の少なくとも二国を指定している特許協力条約 3 6 5 条 (a) 項に基づき国際出願、又は外国での特許出願もしくは発明特許の出願についての外国優先権をここに主張するとともに、優先権を主張している。本出願の前に出願された特許または発明特許の出願出願を以下に、枠内をマークすることで、示しています。

**Prior Foreign Application(s)**

外国での先行出願  
Hei 11-277086

(Number)  
(番号)

Japan

(Country)  
(国名)

(Number)  
(番号)

(Country)  
(国名)

(Number)  
(番号)

(Country)  
(国名)

(Number)  
(番号)

(Country)  
(国名)

私、第 3 5 編米国法典 1 1 9 条 (a) 項に基づいて、下記の米国特許出願規定に記載された権利をここに主張いたします。

(Application No.)  
(出願番号)

(Filing Date)  
(出願日)

私は、下記の米国法典第 3 5 編 1 2 0 条に基づいて下記の特許出願に記載された権利、又は米国を指定している特許協力条約 3 6 5 条 (c) 項に基づき権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第 3 5 編 1 1 2 条第 1 項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第 3 7 編 1 条 5 6 項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

(Application No.)  
(出願番号)

(Filing Date)  
(出願日)

(Application No.)  
(出願番号)

(Filing Date)  
(出願日)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じているところに基づき表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第 1 8 編第 1 0 0 1 条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の表明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

**Priority Not Claimed**

優先権主張なし

29/September/1999

(Day/Month/Year Filed)  
(出願年月日)

☐

(Day/Month/Year Filed)  
(出願年月日)

☐

(Day/Month/Year Filed)  
(出願年月日)

☐

(Day/Month/Year Filed)  
(出願年月日)

☐

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.)  
(出願番号)

(Filing Date)  
(出願日)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Status: Patented, Pending, Abandoned)  
(状況: 特許許可済、係属中、放棄済)

(Status: Patented, Pending, Abandoned)  
(状況: 特許許可済、係属中、放棄済)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration  
(日本語宣言書)

声明状： 私は下記の発明者として、本出願に関する一切の  
手続を米特許庁長官に対して送付する弁護士または代理人  
として、下記の者を指定いたします。（弁護士、または代理  
人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint  
the following attorney(s) and/or agent(s) to prosecute this  
application and transact all business in the Patent and Trademark  
Office connected therewith (last name and registration number)

Michael A. Cantor, Registration No. 31,152; Philmore H. Colburn II,  
Registration No. 35,101; Keith J. Murphy, Registration No. 33,979;  
David A. Fox, Registration No. 38,307; Edward J. Ellis,  
Registration No. 40,389; Robert D. Crawford, Registration No. 38,119

直接送付先

Send Correspondence to:  
Michael A. Cantor, Esq.  
CANTOR COLBURN LLP

55 Griffin Road South  
Bloomfield, CT 06002

直接電話連絡先：（名前及び電話番号）

Direct Telephone Calls to: (name and telephone number)

Edward J. Ellis, Esq.  
(860) 286-2929

第一または第一発明者名	Full name of sole or first inventor Naoaki KOMIYA		
発明者の署名	日付	Inventor's signature	Date
		<i>Naoaki Komiya</i>	Sep. 13, 2000
住所	Residence Ogaki City, Gifu, Japan		
国籍	Citizenship Japan		
私書箱	Post Office Address 1847-1, Miwa-cho, Ogaki City, Gifu, Japan		
第二共同発明者	Full name of second joint inventor, if any Masahiro OKUYAMA		
第二共同発明者	日付	Second inventor's signature	Date
		<i>Masahiro Okuyama</i>	Sep. 13, 2000
住所	Residence Inazawa City, Aichi, Japan		
国籍	Citizenship Japan		
私書箱	Post Office Address 25, Hoden, Kitazima-cho, Inazawa City, Aichi, Japan		